This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-41 (CANCELED)

42. (currently amended) A method of operating a programmable conductor memory device comprising:

storing a binary value as respective ~~complementary~~ resistance states in a first and second programmable conductor memory element wherein the resistance state stored in the first programmable conductor memory element is complementary to the resistance state concurrently stored in the second programmable conductor memory element;

determining a binary value stored in one of said programmable conductor memory elements by discharging respective voltages through said memory elements and comparing the discharging voltages; and

rewriting the binary value stored only in the one of said first and second programmable conductor memory elements which is storing a low resistance state.

43. (currently amended) A method as in claim 42 wherein said discharging comprises:

precharging complementary digit lines to a voltage value; and

respectively discharging the voltage value on each of said complementary digit lines through ~~a respective~~ said first and second programmable conductor memory ~~element~~ elements.

44. (currently amended) The ~~A~~ method as in claim 43 wherein said precharged voltage value on said complementary digit lines is discharged through said respective first and second programmable conductor memory elements by enabling access transistors respectively associated with each of said memory elements.

45. (currently amended) The ~~A~~ method as [[n]] in claim 44 further comprising completing said precharge before enabling said access transistors.

46. (currently amended) The ~~A~~ method as in claim 45 further comprising equilibrating said digit lines before enabling said access transistors.

47. (currently amended) The ~~A~~ method as in claim 44 where said comparison comprises:

determining whether the discharging voltage associated with one memory element is the higher or lower of the two discharging voltages and outputting a first binary value if the discharging voltage associated with the said one memory element is the higher voltage and outputting a second binary value if the discharging voltage associated with said one memory element is the lower voltage.

48. (currently amended) The ~~A~~ method as in claim 47 further comprising setting a digit line having a higher discharge voltage to a first predetermined voltage state and setting a digit line having a lower discharging voltage to a second predetermined voltage state.

49. (currently amended) The ~~A~~ method as in claim 48 wherein said first predetermined voltage is higher than said second predetermined voltage.

50. (currently amended) The ~~A~~ method as in claim 49 wherein said second predetermined voltage is ground voltage.

51. (currently amended) The ~~A~~ method as in claim 48 further comprising disabling said access transistors before said digit lines are set to said first and second voltage states.

52. (currently amended) The ~~A~~ method as in claim 48 further comprising enabling at least one of said access transistors during a time when said digit lines are set to said first and second voltage states.

53-59 (CANCELED)

60. (new) The method as in claim 42, wherein said act of rewriting comprises:

increasing a voltage level of a rowline coupled to said one programmable conductor memory element from approximately ground level to approximately a system voltage level during operation of a sense amplifier circuit used in performing said act of determining.

61. (new) A method of operating a programmable conductor memory device comprising:

storing a binary value as respective resistance states in a first and second programmable conductor memory element wherein the resistance state stored in the first programmable conductor memory element is complementary to the resistance state concurrently stored in the second programmable conductor memory element;

determining a binary value stored in one of said programmable conductor memory elements by discharging respective voltages through said memory elements and comparing the discharging voltages; and

maintaining a voltage level of a wordline coupled to each of said first and second programmable conductor memory elements at approximately ground during activation of a sense amplifier used to perform said act of determining.